Asymmetric Electrical Properties of Corbino a-Si:H TFT and Concepts of Its Application to Flat Panel Displays

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***Abstract*—Inverted stagger hydrogenated-amorphous-silicon (a-Si:H) Corbino thin-film transistors (TFTs) were fabricated with a five-photomask process used in the processing of the active-matrix liquid-crystal displays (AM-LCD). We show that the a-Si:H Corbino TFT has the asymmetric electrical characteristics under different drain-bias conditions. To accommodate for these differences when the electrical device parameters are extracted, we developed asymmetric geometric factors. The ON–OFF current ratio can be significantly enhanced by choosing the outer electrode as the drain, while the field-effect mobility and threshold voltage are identical when different drain-bias conditions are used. Finally, we developed concepts of its possible application to AM-LCDs and active-matrix organic light-emitting displays.**

***Index Terms*—Annular electrode, Corbino, hydrogenated amorphous silicon (a-Si:H), ring-shaped electrode, thin-film transistor (TFT).**

I. Introduction

SINCE Corbino disk was first reported by M. Corbino in 1911 [1], this disk with inner and outer concentric ring contacts has been generally used in magneto-resistance measurement [2] and more recently has also been adopted for organic thin-film-transistor (TFT) structures [3]. In hydrogenated amorphous silicon (a-Si:H) TFT, so called, annular-shape electrode was first introduced in 1996 to provide a reduced gate-to-source capacitance and a smaller photocurrent level in active-matrix liquid crystal displays (AM-LCDs) [4]. In 1999, to characterize the electrical properties of the silicon-on-oxide wafers by device geometrical factors, ring-shaped and circular electrodes were used in the pseudometal-oxide-semiconductor field-effect transistor (Ψ-MOSFET) [5]. Recently, in silicon-based CMOS, annular MOSFET with the concentric circular boundaries was designed to enhance the device electrical reliability by modulating the electric field at the drain end of the channel [6]. So far, the detailed discussion of the geometrical effects of Corbino electrodes on a-Si:H TFT electrical properties and its possible application to flat panel displays has not been provided.

In this paper, first, we report on Corbino a-Si:H TFT's asymmetric electrical characteristics. More specifically, we studied the effects of the drain-bias polarity on the Corbino TFT's electrical properties. We also investigated the a-Si:H TFT geometrical effects on the extraction of key device electrical parameters such as subthreshold slope, field-effect mobility, and threshold voltage, that are important for AM-LCDs and active-matrix organic light-emitting devices (AM-OLEDs). Then, we discuss the possible uses of this device in AM-OLEDs as a driving TFT. To the best of our knowledge, this paper represents the first investigation of the a-Si:H Corbino TFT asymmetric electrical characteristics and their impact on AM-LCDs and AM-OLEDs.

II. Corbino a-Si:H TFT Fabrication

The Corbino a-Si:H TFT is consisting of circle-shape inner electrode (radius $R_1 = 12\ \mu$m) and ring-shaped outer electrode (inner radius $R_2 = 18\ \mu$m), as shown in Fig. 1. The bottom gate electrode is large enough to cover the entire area of the device's outer and inner electrodes. The Corbino a-Si:H TFT was fabricated using the normal AM-LCD five-photomask process steps [7]. More specifically, on the Corning Eagle2000 glass substrate, a bilayer of aluminum–neodymium compound (AlNd, 2000 Å) and molybdenum (Mo, 500 Å) was deposited by a sputtering method. The Mo/AlNd gate electrode was then patterned by wet etching (Mask #1). Following the gate-electrode definition, hydrogenated amorphous silicon nitride (a-SiN$_X$:H, 4000 Å)/a-Si:H (1700 Å)/phosphorus-doped a-Si:H (n^+ a-Si:H, 300 Å) trilayer was deposited by plasma-enhanced chemical vapor deposition (PECVD) at 350 °C to form a gate insulator and active channel layer, respectively. After defining the device active island by reactive ion etching (RIE) (Mask #2), a chromium (Cr, 1200 Å) layer was deposited by sputtering, and the source/drain (S/D) electrodes were patterned by wet etching (Mask #3). Using the same photo-resist over S/D metal as masks, the back-channel-etching by RIE was performed. Then, we deposited a-SiN$_X$:H (3000 Å) as a passivation layer by PECVD at 300 °C. To make a contact for the indium tin oxide (ITO) pixel electrode, via was formed through the passivation (PVX) layer by RIE (Mask #4). After contact via definition, ITO (500 Å) was deposited by a sputtering method at room temperature, and then the pixel electrodes

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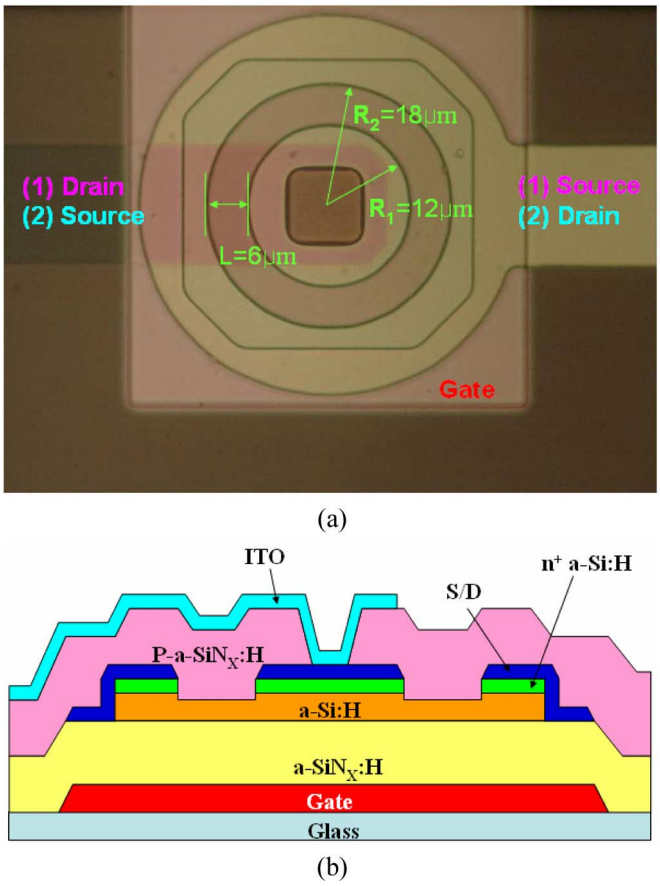

Fig. 1. (a) Top view and (b) cross section of the Corbino a-Si:H TFT device.

were patterned by wet etching (Mask #5). As a final step, the thermal annealing of ITO and TFT was performed for 1 h at 235 °C. The schematic representation of the cross section of Corbino a-Si:H TFT structure is shown in Fig. 1(b).

III. Experimental Results

To characterize the electronic properties of the Corbino a-Si:H TFT, we first measured the output characteristics, as shown in Fig. 2, by applying the drain bias under the following conditions.

1) Ground was applied on the outer ring source electrode, and drain voltage was applied on the inner circle drain electrode.
2) Drain voltage was applied on the outer ring drain electrode, and ground was applied on the inner circle source electrode.

We swept the drain bias from 0 to 40 V for various gate voltages (0, 10, and 20 V). As shown in Fig. 2, at $V_{\rm DS} = 20$ V and $V_{\rm GS} = 20$ V, the output current for condition 1) ($= 11.8\ \mu$A) is 1.73 times higher than for condition 2) ($= 6.82\ \mu$A).

Next, we measured the transfer characteristics of Corbino a-Si:H TFT; we swept the gate bias from 15 to -5 V and swept again from -5 to 15 V for various drain voltages (0.1, 1, 10, and $V_{\rm SAT}$, where $V_{\rm SAT}$ is the drain voltage when $V_{\rm DS} = V_{\rm GS}$). As shown in Fig. 3, at low drain voltage ($V_{\rm DS} =$ 0.1 V), the ON currents are identical for both conditions. However, at high $V_{\rm DS}(> 1$ V), the ON currents for condition 1)

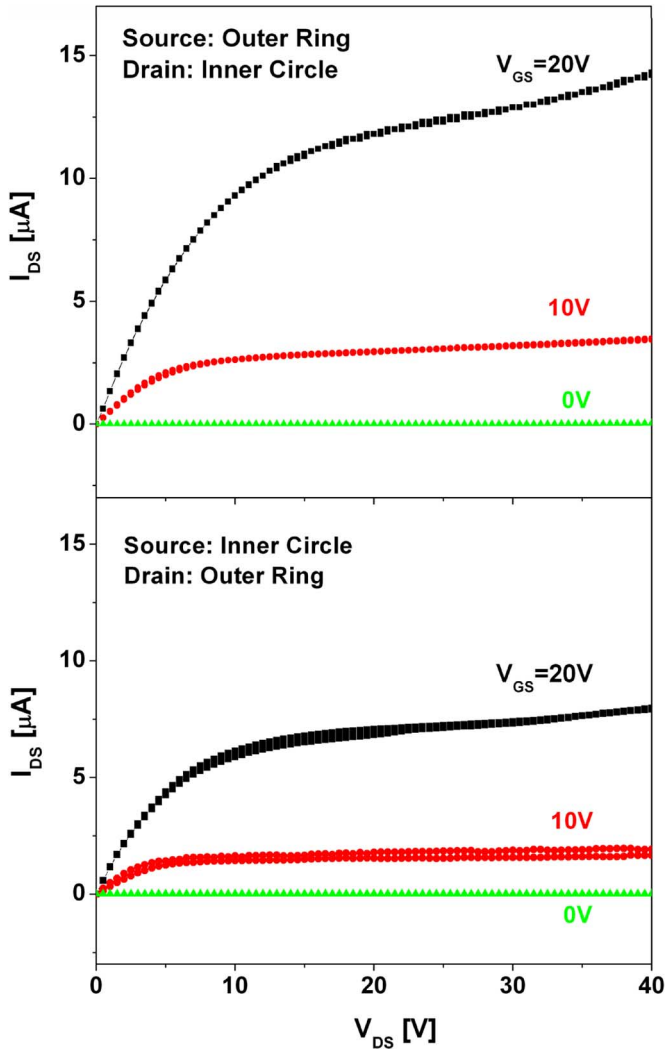

Fig. 2. Output characteristics of the Corbino a-Si:H TFT for the two drain-bias conditions defined in the text.

are higher than for condition 2). Therefore, regardless of the gate bias and direction of the drain bias applied, the ON currents would be the same for a low drain bias. However, when we apply a high drain bias, the ON current levels can be increased significantly depending on the drain-bias direction. At the same time, as the drain bias is increased from 0.1 to 10 V, the OFF current for condition 2) increases from $\sim 10^{-14}$ to $\sim 10^{-12}$ A, while the OFF current for condition 1) remains low (from $\sim 10^{-14}$ to $\sim 10^{-13}$ A). During gate-bias sweeping, no significant hysteresis in current–voltage characteristics was observed for both conditions; at $V_{\rm DS} = 10$ V and $I_{\rm DS} = 0.1$ nA, both conditions showed gate voltage variation ($\Delta V_{\rm GS} =$ $0.3\ {\rm V}_{\rm condition\ 1)}, 0.55\ {\rm V}_{\rm condition\ 2)}$) acceptable for AM-LCDs.

IV. Discussions of a-Si:H TFT Geometry Effect

The asymmetric behaviors of the Corbino a-Si:H TFT described above can be explained as follows. As the gate bias increases, a channel is formed in the active a-Si:H layer at the interface with the gate insulator. At low $V_{\rm DS}$ ($\sim$1 V), since the channel is not highly affected by the drain voltage, the whole channel layer can be considered as the carrier accumulation

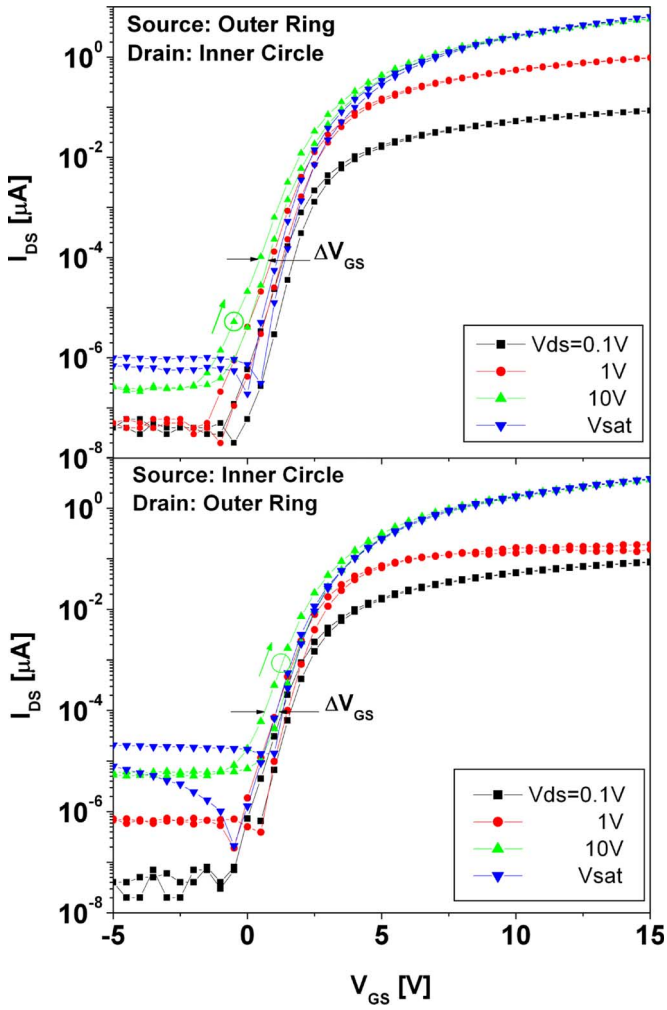

Fig. 3. Transfer characteristics of the Corbino a-Si:H TFT for the two drain-bias conditions defined in the text.

layer. Hence, effectively, the shape and length of the channel would be the same for both drain-bias polarities.

Considering the geometrical effect of the channel on the drain–current, we adopted to the Corbino a-Si:H TFT the analytical model developed for Ψ-MOSFET [5]. The drain–current is assumed to be constant at distance r from the inner circle and can be expressed as $I_D = 2\ \pi r J_r$, where the current density J_r is a function of radial electric field E_r and potential V_r : $J_r = \sigma E_r = \sigma dV_r/dr$. The resulting differential equation for the potential is expressed as

$$dV = \frac{I_D}{2\pi\sigma} \cdot \frac{1}{r} dr \tag{1}$$

where dark conductivity $\sigma = \mu C_{\rm OX}[(V_{\rm GS} - V_{\rm TH}) - V_r]$, and μ is the field-effect mobility, $C_{\rm OX}$ is the oxide capacitance, $V_{\rm GS}$ is the gate bias, and $V_{\rm TH}$ is the threshold voltage of TFT. The integration of (1) from R_1 to R_2 yields the potential drop between the source and the drain electrodes as

$$\int_0^{V_{\rm DS}} \left[(V_{\rm GS} - V_{\rm TH}) - V_r\right] dV_r = \frac{I_D}{2\pi\mu C_{\rm OX}} \int_{R_1}^{R_2} \frac{1}{r} dr. \tag{2}$$

Hence, the drain–current for both drain-bias polarity can be expressed as

$$I_D = f_{g0}\mu C_{\rm OX}\left[(V_{\rm GS} - V_{\rm TH})V_{\rm DS} - V_{\rm DS}^2/2\right]$$
$$\text{where} \quad f_{g0} = \frac{2\pi}{\ln(R_2/R_1)}. \tag{3}$$

Thus, instead of using the middle circumference of the Corbino a-Si:H TFT as the device effective width $W_{\rm eff} = \pi(R_1 + R_2)$, the geometrical factor f_{g0} should be used for both drain-bias conditions during extraction of the device field-effect mobility and threshold voltage at low $V_{\rm DS}$ (linear regime).

However, the output and transfer characteristics at high $V_{\rm DS}$ ($>$ 10 V) are quite different from those measured at a low $V_{\rm DS}$. As discussed above, at high $V_{\rm DS}$, the ON current is higher for drain-bias condition 1) than drain-bias condition 2). If we assume that the device is an ideal crystalline silicon MOSFET and the field-effect mobility remains identical for both bias conditions, the current flowing through TFT can only be dependent on the value of the channel width and the length. Therefore, at high $V_{\rm DS}$, we need to define the different geometrical factor f_g for each drain-bias condition to accommodate for the differences in device electrical properties. When TFT is operating in the saturation regime at high $V_{\rm DS}$, we assume that the channel depletion region at the drain electrode would increase by a certain value. This change is referred to as channel length modulation factor (ΔL). In the Corbino a-Si:H TFT, due to the unique device geometry, we can expect that ΔL would be different depending on the drain-bias condition or the position of drain and source electrodes [8]. If the drain bias fully depletes the channel by ΔL from the edge of the drain electrode, the electric field at the depletion region edge can be expressed by Gauss' law; the charge contained in a volume (ρ) equals to the permittivity $(\varepsilon_{\text{a-Si}})$ of a-Si:H times the electric field emanating from the volume

$$\oint \rho dV = \varepsilon_{\text{a-Si}} E. \tag{4}$$

If the drain bias creates the same number of the depletion-region charge per unit volume (Q_d) for both drain-bias conditions, the electric field for each condition can be expressed by

$$E_1 \cong \frac{\left(Q_d \times x_i \times \pi(R_1 + \Delta L_1)^2\right)}{\varepsilon_{\text{a-Si}}} \tag{5a}$$

$$E_2 \cong \frac{\left[Q_d \times x_i \times \pi\left((R_2 + W_R + \Delta L_2)^2 - (R_2 + \Delta L_2)^2\right)\right]}{\varepsilon_{\text{a-Si}}} \tag{5b}$$

where x_i is the depletion width of the drain depletion region, and W_R is the width of the outer ring electrode. If the electric field across the drain depletion region is the same for both bias conditions $(E_1 = E_2)$, since the size of the drain electrode is larger for condition 2) than for condition 1) $(2\pi R_2 > 2\pi R_1)$,

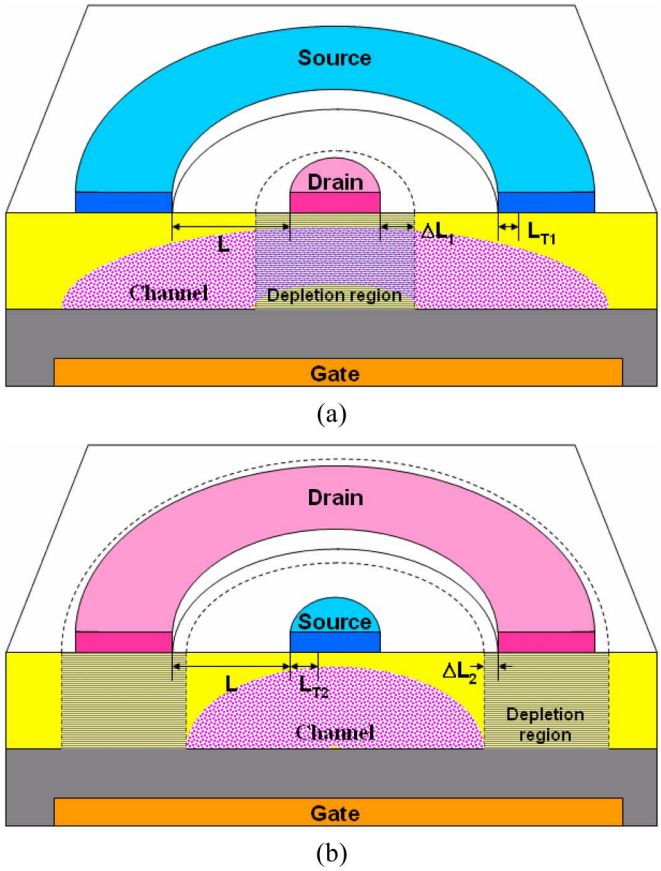

Fig. 4. Cross sections of the Corbino a-Si:H TFT and the schematic representation of the depletion region formation for two drain-bias conditions. (a) Drain bias is applied on the inner circular electrode. (b) Drain bias is applied on the outer ring electrode.

the depletion region at the drain side for condition 1) is expected to be larger than for condition 2) ($\Delta L_1 > \Delta L_2$), as shown in Fig. 4(a) and (b). It should be noted that due to the unique bottom-gate Corbino TFT structure, the formed channel is expected to extend even below the source electrode, as shown in Fig. 4. However, it is well known that in a-Si:H TFT, the drain–current does not flow through the whole source electrode length but is rather limited to a specific length, which is the so-called TFT characteristic length (L_T) [9] near the electrode edge. Hence, the characteristic length for each drain-bias condition can be defined as L_{T1} and L_{T2}, respectively. To estimate the L_{T1} and L_{T2}, we measured the channel resistance ($r_{\rm ch}$) and S/D contact resistance ($R_{\rm S/D}$) for the four Corbino TFTs with different channel lengths for each drain-bias condition. From the measurements, the TFT characteristic length ($= R_{\rm S/D}/r_{\rm ch}$) was calculated as 2 μm ($= L_{T2}$) and 1 μm ($= L_{T1}$) at $V_{\rm GS} = 15$ V, respectively. From the experimental results, we can speculate that L_{T2} is larger than L_{T1} because the size of the electrode acting as an electron source is smaller for drain-bias condition 2) than for drain-bias condition 1).

Based on these assumptions, to derive the equation for the drain–current in the saturation regime, the same methodology was applied here as the one used for the derivation of (1); the integration of (2) from $R_1 + \Delta L_1$ to $R_2' (= R_2 + L_{T1})$ for drain-bias condition 1) and from $R_1' (= R_1 - L_{T2})$ to $R_2 - \Delta L_2$ for drain-bias condition 2) yields the potential drop between the source and drain electrodes for each case, respectively

$$\int_0^{V_{\rm DS}} [(V_{\rm GS} - V_{\rm TH}) - V_r]\, dV_r = \frac{I_D}{2\pi\mu C_{\rm OX}} \int_{R_1+\Delta L_1}^{R_2'} \frac{1}{r} dr \quad (6a)$$

$$\int_0^{V_{\rm DS}} [(V_{\rm GS} - V_{\rm TH}) - V_r]\, dV_r = \frac{I_D}{2\pi\mu C_{\rm OX}} \int_{R_1'}^{R_2-\Delta L_2} \frac{1}{r} dr. \quad (6b)$$

To find the values for ΔL_1 and ΔL_2 and the corresponding equations for the asymmetric drain–current, we have done the asymmetric current calculation of Corbino a-Si:H TFT based on the standard TFT with the same length as reference [width $(W) = 60$ μm and length $(L) = 6$ μm]. The output drain–current of conventional standard TFT was measured at $V_{\rm GS} = 20$ V and then normalized with its width-over-length ratio $(W/2L)$, to be used as a reference value for the current calculation. Since both Corbino and standard a-Si:H TFT have been fabricated over the same substrate at the same time, we expect that their normalized electrical properties are equivalent, and only the geometries are different. Using a normalized output drain–current of standard TFT, we calculated the output drain–current of Corbino TFT for each bias condition by multiplying the normalized standard TFT characteristic by the geometric factors defined in (7) (output current of Corbino TFT = normalized output current of standard TFT $\times$ geometrical factor). By fitting several different values of ΔL_1 and ΔL_2 onto the integrations above, we could find proper values for the channel length modulation factors empirically as $\Delta L_1 = L/6$ for condition 1) and $\Delta L_2 = L/10$ for condition 2), respectively. Hence, since $V_{\rm DS} = (V_{\rm GS} - V_{\rm TH})$ in the saturation regime, the drain–current for each condition can be expressed with the corresponding geometrical factors f_{g1} and f_{g2}

$$I_D^{\rm Condition\,1)} = f_{g1}\mu C_{\rm OX}(V_{\rm GS} - V_{\rm TH})^2$$
$$\text{where} \quad f_{g1} = \frac{\pi}{\ln\left[6R_2'/\left(R_1 + 5R_2'\right)\right]} \quad (7a)$$

$$I_D^{\rm Condition\,2)} = f_{g2}\mu C_{\rm OX}(V_{\rm GS} - V_{\rm TH})^2$$
$$\text{where} \quad f_{g2} = \frac{\pi}{\ln\left(\left(9R_2 + R_1'\right)/10R_1'\right)}. \quad (7b)$$

As shown in (7), in the saturation regime, the values of the geometrical factors can have direct impact on the drain–current values. When R_1 and R_2 in (7) are replaced with the actual measured values ($R_1 = 18$ μm and $R_2 = 12$ μm), the geometrical factor in condition 1) turns out to be larger than in condition 2) by about 1.6 times. Therefore, the ON current for the drain-bias condition 1) is expected to be larger than for drain-bias condition 2) by the difference in the geometrical factors. As shown in Fig. 5, we could exactly match the measured output drain–current of Corbino TFT for each drain-bias condition. It should be noted that when the intuitive channel width [$W_{\rm EFF1} = 2\,\pi R_2$ for condition 1) and $W_{\rm EFF2} = 2\,\pi R_1$ for condition 2)] is used as the circumference of the source electrode instead of the geometrical factors given

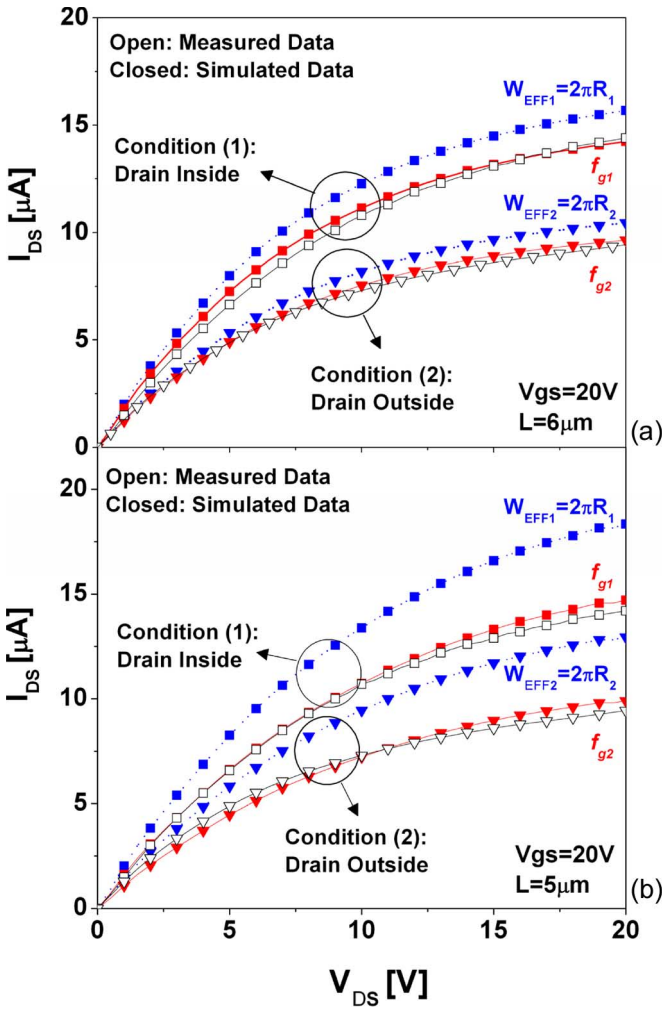

Fig. 5. Measured (open symbol) and calculated (closed symbol) output characteristics of the Corbino a-Si:H TFT. (a) $R_2 = 18$ μm, and $R_1 = 12$ μm. (b) $R_2 = 17$ μm, and $R_1 = 12$ μm.

by (7), the calculated drain–current values are much larger than the experimental values, as shown in Fig. 5(a). To validate these equations of geometrical factor, we measured another set of Corbino and standard TFTs with different dimensions: $R_1 = 17$ μm and $R_2 = 12$ μm for the Corbino TFT and $W = 60$ μm, and $L = 5$ μm for the standard TFT. Again, the standard TFT to be used as a reference for the calculated drain–current is normalized by $W/2L$. As shown in Fig. 5(b), although there is a little deviation observed for drain-bias condition 1), the measured output drain–current of Corbino TFT could only be exactly matched when the normalized drain–current of standard TFT is multiplied for each bias condition by the defined geometrical factor in (7). Again, when the intuitive channel width [$W_{\mathrm{EFF1}} = 2\,\pi R_2$ for condition 1) and $W_{\mathrm{EFF2}} = 2\,\pi R_1$ for condition 2)] is used instead of the geometrical factor, the calculated output drain–current of Corbino TFT shows a large difference from the measured values!

The OFF current in a-Si:H TFT is originated from the carriers generated in the depletion region on the drain side (at high V_{DS}) when negative gate bias is applied. Under $V_{\mathrm{GS}} < 0$, the a-Si:H is fully depleted, and hole accumulation will take place near the a-Si:H/a-SiN$_X$:H interface creating a hole current. The current level is limited by the n$^+$-a-Si:H S/D contact regions (these are hole blocking contacts). If we assume that two quasi-n$^+$-p junctions are formed between the drain and source n$^+$-regions and hole (p) conduction channel, the drain n$^+$-p junction is under reverse bias ($V_{\mathrm{DS}} > 0$), which is similar to an n$^+$-p junction in the OFF state. Indeed, in a regular n$^+$-p junction, the OFF current is carried by a minority carrier generated in the depletion region. The OFF current (J_g) in this region can be limited by the generation rate of carriers and the depletion width x_i as shown in the following equation:

$$J_g = \frac{qn_i x_i}{2\tau_0} \tag{8}$$

where q is the electron charge, n_i is the maximum generation rate, and τ_0 is the lifetime of excess carrier in the depletion region. If we assume that the width of the depletion region and the generation rate are identical for both drain-bias conditions at high V_{DS}, the OFF current can depend only on the volume of the depletion region (= the area of drain electrode × the depletion width x_i) for each bias condition. Therefore, since the area of drain electrode is larger in drain-bias condition 2) than in drain-bias condition 1), the OFF current for condition 2) is expected to be much higher than for condition 1).

V. Device Parameters Extraction

From the TFT data shown in Figs. 2, 3, and 6, we can extract the subthreshold slope (S), threshold voltage, and field-effect mobility values. We chose the center position (at $I_{\mathrm{DS}} = 10^{-10}$ A) in the transfer curve of log (I_D) versus V_{GS} and use the linear fitting by taking two log (I_D) values around the center point to extract the S-value.

The field-effect mobility (μ) and threshold voltage can be calculated as follows: From the transfer curve of I_D versus V_{GS} (Fig. 6), we chose a specific value of I_D at $V_{\mathrm{GS}} = 15$ V. By taking 90% and 10% of this selected I_D value, we define the fitting range in I_D versus V_{GS} experimental characteristics. From the slope and x-axis intercept of the calculated curve, the field-effect mobility and threshold voltage have been extracted using (3) and (7) with different geometrical factors. Calculated device parameters are summarized in Table I(a) for linear (low V_{DS}) and saturation (high V_{DS}) regions, respectively. For the comparison, we also calculated field-effect mobility (μ) and threshold voltage by using the maximum slope method [10] which is usually used for crystalline silicon devices. Fig. 6 shows variations of transconductance ($= dI_{\mathrm{DS}}/dV_{\mathrm{GS}}$) for each drain-bias condition as a function of gate bias for linear (low V_{DS}) and saturation (high V_{DS}) regions, respectively. The field-effect mobility is calculated from transconductance maximum (g_m) value using the following equations:

$$\mu_{\mathrm{Linear}} = \frac{g_{m\text{-Linear}}}{f_g C_{\mathrm{OX}} V_{\mathrm{DS}}} \tag{9a}$$

$$\mu_{\mathrm{Saturation}} = \frac{g^2_{m\text{-Saturation}}}{f_{g1,2} C_{\mathrm{OX}}} \tag{9b}$$

where $g_{m\text{-Linear}}$ is the maximum transconductance at $V_{\mathrm{DS}} = 0.1$ V, and $g_{m\text{-Saturation}}$ is the maximum transconductance at

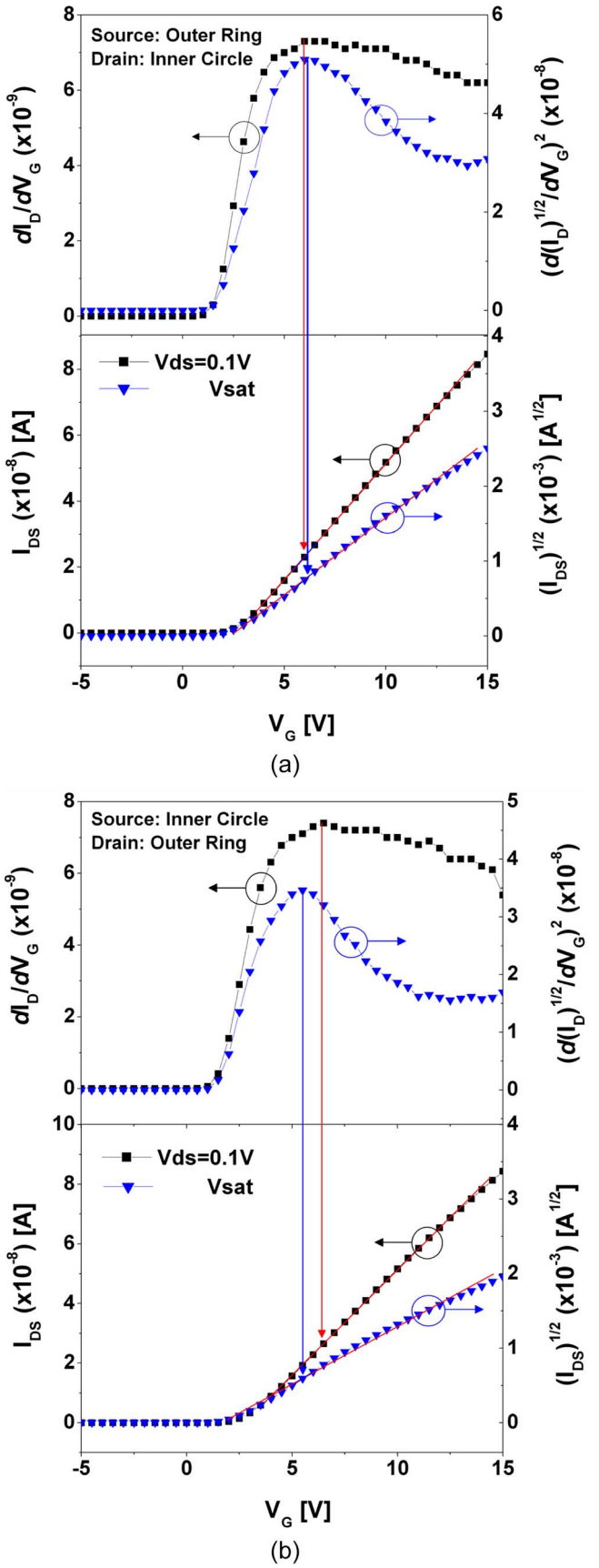

Fig. 6. Transconductance and corresponding transfer characteristics of the Corbino a-Si:H TFT. Curves used for the extraction of the threshold voltage and mobility are also shown. (a) Drain bias is applied on the inner circular electrode. (b) Drain bias is applied on the outer ring electrode.

$V_{\mathrm{DS}} = V_{\mathrm{SAT}}$. From the V_{GS} value corresponding to the g_m as a reference, two closest different gate-bias values are chosen so that the straight fitting line is drawn through these three points in the transfer characteristic curves. The threshold voltage can be estimated from the x-axis intercept of this extrapolated line for each drain-bias condition, as shown in Fig. 6. Resulting extracted parameters are summarized in Table I(b). It is clear from this table that those two calculation methods provide very similar mobility and threshold-voltage values for Corbino a-Si:H TFTs (within experimental error). Fig. 7 shows the evolution of field-effect mobility with the gate bias (9) for each drain-bias condition. In linear regime operation ($V_{\mathrm{DS}} =$ 0.1 V), the field-effect mobility rises very fast from around the threshold voltage and saturates with the gate bias for both drain-bias conditions, as observed in normal MOSFET. In saturation regime operation ($V_{\mathrm{DS}} = V_{\mathrm{SAT}}$), the field-effect mobility again rises very fast from around the threshold voltage but decreases with the gate bias due to the scattering effect within the channel layer.

As shown in the table, due to a lower OFF current, the sub-threshold slope is much lower for the drain-bias condition 1), while the field-effect mobility and threshold voltage are similar for both bias conditions. Therefore, asymmetric biasing of the Corbino a-Si:H TFT can change the ON- and OFF-current ratios, while the field-effect mobility and threshold voltage remain the same, regardless of the drain-bias conditions. This enhanced ON–OFF current ratio has an advantage when the device is used as a driving device for AM-OLEDs where the constant current should be applied to OLED with the minimum leakage current during display operation.

Since the ring-shaped electrode provides a uniform electric-field distribution in the channel region and eliminates any local electric-field crowding due to sharp corners present in normal TFT, Corbino TFT is expected to have not only larger W/L ratio but also a better electrical stability in comparison to the normal standard TFTs. This topic will be addressed in more details in the future publications [11]. Finally, to reduce the pixel-electrode parasitic capacitances, the gate electrode can be patterned into a ring shape to be localized beneath the source and drain contact regions.

VI. Possible Applications of Corbino a-Si:H TFTs to Flat Panel Displays

It is possible to use the Corbino a-Si:H TFT for flat-panel-display applications. Fig. 8(a) and (b) presents schematic top views and cross sections of the Corbino a-Si:TFT use as a switching TFT for conventional AM-LCDs and a driving TFT for AM-OLEDs, respectively. The storage capacitor is not taken into consideration in these simple pixel-electrode schematics. When the device is used as a switching TFT, as shown in Fig. 8(a), with the minimized overlapped area between the gate and source electrode when the pixel electrode is patterned, Corbino TFT has an advantage of having a much smaller parasitic gate-to-source capacitance (C_{GS}) than a normal TFT [4]. This will provide a minimum pixel-voltage drop (error voltage) due to the C_{GS} with the gate pulse in the OFF state. By achieving a low error voltage, the a-Si:H TFT AM-LCD optical

TABLE I
EXTRACTED PARAMETERS OF THE CORBINO a-Si:H TFT BY USING THE (a) STANDARD AND (b) MAXIMUM SLOPE METHODS; CONDITION (1) IS DEFINED FOR THE DRAIN BIAS APPLIED ON THE INNER CIRCULAR ELECTRODE, AND CONDITION (2) IS DEFINED FOR THE DRAIN BIAS APPLIED ON THE OUTER RING ELECTRODE

(a)	V_{DS}=0.1V		V_{DS}=V_{sat}	
Condition	(1)	(2)	(1)	(2)
S [mV/Dec]	488	532	416.6	538
V_{th} [V]	2.6	2.7	2.6	2.2
μ [cm^2/V·s]	0.31[a)]	0.32[a)]	0.37[b)]	0.36[c)]

(b)	V_{DS}=0.1V		V_{DS}=V_{sat}	
Condition	(1)	(2)	(1)	(2)
V_{th} [V]	2.6	2.7	2.7	2.3
μ [cm^2/V·s]	0.32[a)]	0.32[a)]	0.39[b)]	0.42[c)]

Geometrical factor a) f_{g0}, b) f_{g1}, and c) f_{g2} is used to extract the parameter.

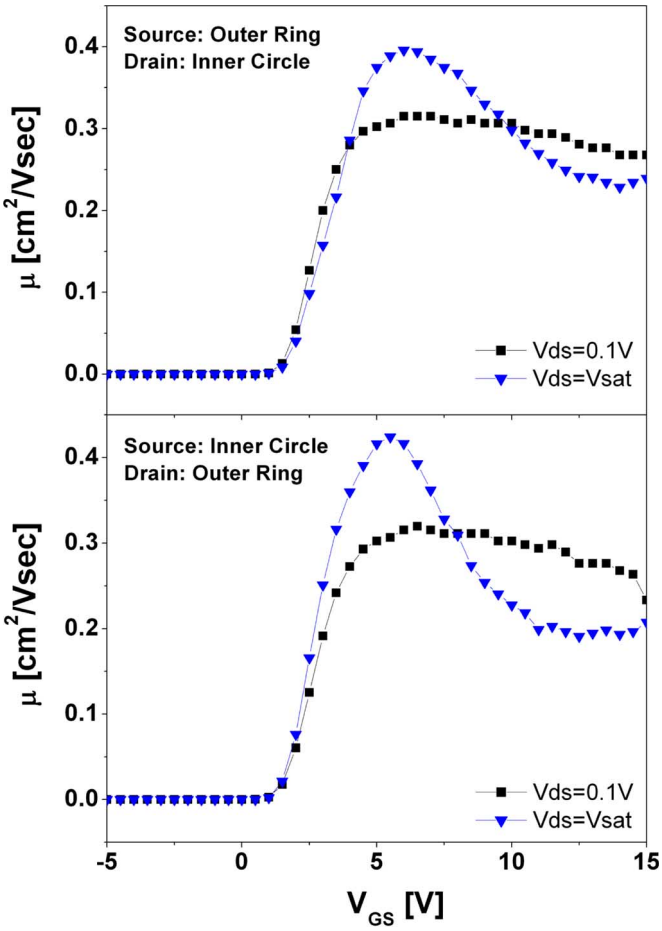

Fig. 7. Variation of the field-effect mobility of the Corbino a-Si:H TFT as a function of gate bias.

quality can be improved; the flicker noise can be suppressed [12]. However, in an AM-LCD driving scheme, the polarity of the data line bias usually changes from line-to-line with respect to the common (line inversion method); hence, the positions of the drain and the source in TFT should be opposite in odd and even data lines. In such case, as mentioned above, TFTs in the AM array will have different ON- and OFF-current values for different lines. Since the ON current is only used for charging the storage capacitor, asymmetric ON current will not affect the storage capacitor voltage as long as the TFT switch turn-on time is long enough to allow full pixel charging. The TFT switch turn-off time is relatively very long compared with the TFT switch turn-on time in AM-LCD operation. Therefore, due to the asymmetric OFF-current behavior of Corbino a-Si:H TFT, stored charges in storage capacitor may vary between lines, which could cause a dramatic change in the storage capacitor voltage. Such change can cause the difference in the light transmittance of liquid crystal and create a possible line MURA defect in AM-LCD [13].

Fig. 8(b) shows a possible application of the Corbino a-Si:H TFT to AM-OLEDs as a driving transistor (only two simple TFTs pixel-electrode circuits are considered here); the top light-emitting anode OLED is used in this pixel circuit. Here, the switching TFT structure is identical to a switching TFT in AM-LCDs. Pixel electrode is, however, made of aluminum (Al) or aluminum alloy coated with a thin metal layer such as magnesium (Mg) or calcium (Ca) instead of ITO since this layer is used as a cathode in OLED; other cathode-electrode structures could also be used. Then, the electron-transporting layer, organic light-emissive layer, and hole-transporting layer are deposited successively over the cathode electrode. Finally, a transparent thin metal oxide (WO_3 or MoO_3)/ITO or Al bilayer is deposited as an anode to form a top light-emitting anode OLED structure. In AM-OLED, the gate of driving n-channel TFT should always be turn-on to supply constant current flowing to OLED. Therefore, the pixel voltage is not likely to be affected by the gate-to-drain capacitance of TFT, and we can extend the area of pixel electrode to maximize the pixel aperture ratio. In addition, since the positions of the source and drain are always fixed in driving TFT, we can enhance the ON- and OFF-current ratio and minimize the OFF current by using the outer ring electrode as the source in Corbino a-Si:H TFTs. At the same time, such device design provides flexibility to realize a high W/L ratio needed to achieve a high ON-current level. Finally, as mentioned above, we expect that such device will have better electrical stability in comparison to the normal TFT structure.

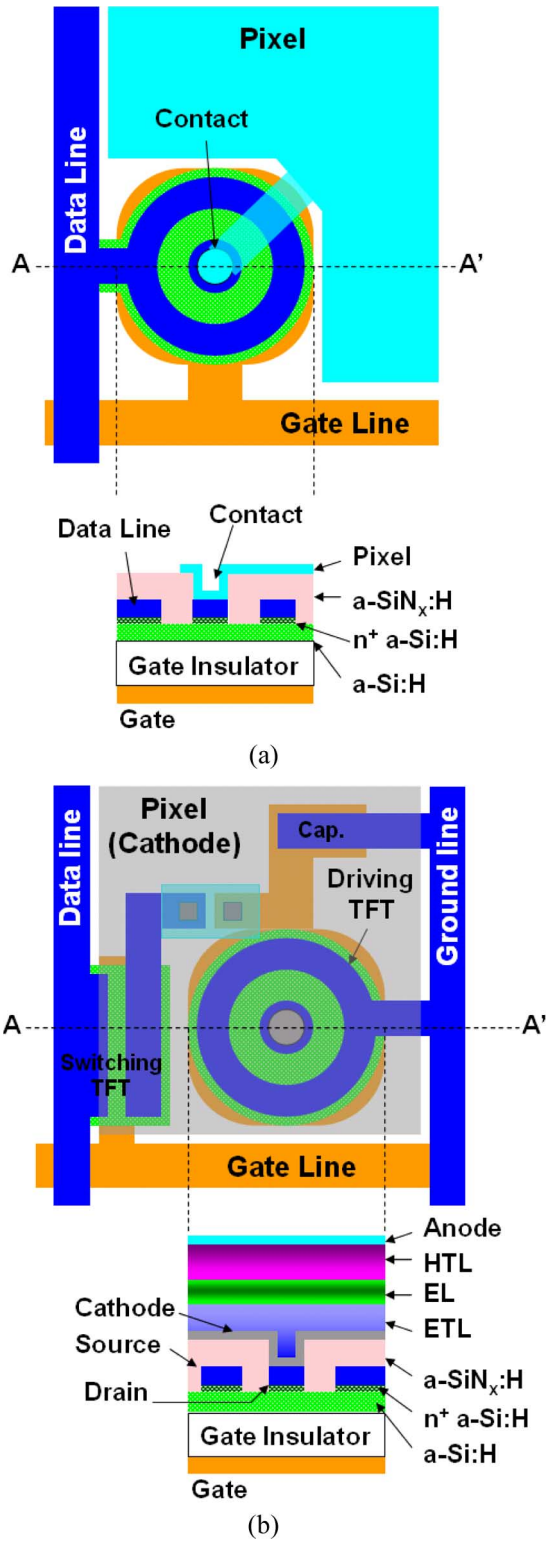

Fig. 8. Top views and cross sections of the proposed Corbino a-Si:H TFT pixel electrodes for (a) AM-LCD and (b) AM-OLED.

VII. Conclusion

In this paper, we have studied the asymmetric electrical characteristics of Corbino a-Si:H TFT associated with the different drain-bias conditions. Due to unique Corbino disk geometry, when the source is connected to the outer ring electrode, the ON current is about two times higher, and the OFF current is about ten times lower than when the source is applied to the inner circle electrode at high drain voltages (> 10 V). However, the threshold voltage and the field-effect mobility remain the same for both drain-bias conditions.

We also found that the Corbino a-Si:H TFT might not be an adequate switching device for AM-LCD due to the asymmetric OFF-current behavior; the leakage current would vary depending on the drain-bias condition. However, at the same time, owing to its high ON current and possible enhanced electrical stability, the Corbino a-Si:H TFT is a good candidate to be used as a driving TFT for top light-emitting anode AM-OLEDs.

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References

[1] D. A. Kleinman and A. L. Schawlow, "Corbino disk," *J. Appl. Phys.*, vol. 31, no. 12, pp. 2176–2187, Dec. 1960.
[2] C. Schierholz, R. Kürsten, G. Meier, T. Matsuyama, and U. Merkt, "Weak localization and antilocalization in the two-dimensional electron system on p-type InAs," *Phys. Stat. Sol. B*, vol. 233, no. 3, pp. 436–444, 2002.
[3] H. Klauk, D. J. Gundlach, J. A. Nichols, and T. N. Jackson, "Pentacene organic thin-film transistors for circuit and display applications," *IEEE Trans. Electron Devices*, vol. 46, no. 6, pp. 1258–1263, Jun. 1999.
[4] Y. H. Byun, W. D. Boer, M. Yang, and T. Gu, "An amorphous silicon TFT with annular-shaped channel and reduced gate-source capacitance," *IEEE Trans. Electron Devices*, vol. 43, no. 5, pp. 839–841, May 1996.
[5] D. Munteanu, S. Cristoloveanu, and H. Hovel, "Circular pseudo-metal oxide semiconductor field effect transistor in silion-on-insulator," *Electrochem. Solid-State Lett.*, vol. 2, no. 5, pp. 242–243, May 1999.
[6] D. C. Mayer, R. C. Lacoe, E. E. King, and J. V. Osborn, "Reliability enhancement in high-performance MOSFETs by annular transistor design," *IEEE Trans. Nucl. Sci.*, vol. 51, no. 6, pp. 3615–3620, Dec. 2004.
[7] D. Pribat, "The use of thin silicon films in flat panel displays," *Mater. Sci. Forum*, vol. 455, pp. 56–63, 2004.
[8] E. F. Girczyc and A. R. Boothroyd, "A one dimensional DC model for nonrectangular IGFET's," *IEEE J. Solid-State Circuits*, vol. SSC-18, no. 6, pp. 778–784, Dec. 1983.
[9] C. R. Kagan and P. Andry, *Thin-Film Transistors*. New York: Marcel Dekker, 2003.
[10] Y. P. Tsividis, *Operation and Modeling of the MOS Transistor*. New York: McGraw-Hill, 1987.
[11] H. Lee, J. S. Yoo, C. D. Kim, I. J. Chung, and J. Kanicki, *Electrical Stability of a-Si:H Corbino TFT for AM-OLED Displays,* to be submitted for publication.
[12] Y. Kaneko, Y. Tanaka, N. Kabuto, and T. Tsukada, "A new address scheme to improve the display quality of a-Si TFT/LCD panels," *IEEE Trans. Electron Devices*, vol. 36, no. 12, pp. 2949–2952, Dec. 1989.
[13] W. K. Pratt, S. S. Sawkar, and K. O'Reilly, "Automatic blemish detection in liquid crystal flat panel displays," *Proc. SPIE*, vol. 3306, pp. 2–13, Feb. 1998.

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